Wednesday, May 10 2023

9:00-9:45 Registration

9:45-10:00 Conference opening

10:00-10:45 Invited talk

Ehrenfried Seebacher, "Semiconductor Devices for Integrated Optical Solutions". ams-OSRAM (Austria)

10:45-11:00 Coffee break

11:00-12:00 Session 1. Noise. Chair: Bogdan Cretu

11:00.11:20 R. Asanovski (*Università degli Studi di Modena e Reggio Emilia. Italy*). Characterization of DC Performance and Low-Frequency Noise of an Array of nMOS Forksheets from 300 K to 4 K

11:20-11:40 E. Simoen (*Ghent University. Belgium*). 3D Backside Integration of FinFETs: Is there an impact on LF Noise?

11:40-12:00 L. Van Brandt (*UCLouvain, ICTEAM.Belgium*). "On Noise-Induced Transient Bit Flips in Subthreshold" SRAM

12:00-13:00 Session 2. Compound semiconductor devices. Chair: E. Sangiorgi

12:00-12:20 A. Zaslavsky (*Brown University. USA*). GaN hot electron transistors: From ballistic to coherent

12:20-12:40 W. Perina (*University of Sao Paulo. Brazil*). Experimental Study of MISHEMT from 450 K down to 200 K for analog applications

12:40-13:00 T. Spelta (*CEA LETI. France*). Impact of etching process on Al2O3/GaN interface for MOSc-HEMT devices combining ToF SIMS, HAXPES and AFM

13:00-14:00 Lunch

14:00-16:05 Session 4. Poster session (Room: Sala de Juntes)

1. ONLINE - S. Srivastava (*S.V. National Institute of Technology, Surat. India*). Understanding the Impact of Extension Region on Stacked Nanosheet FET: Analog Design Perspective
2. ONLINE - L. C. Acharya (*Indian Institute of Technology, Roorkee. India*). Prediction of Variation Aware FOSC in Ring Oscillators (ROs) to Mitigate Aging Impact on RO-PUF
3. ONLINE - Shashidara M (*Sardar Vallabhbhai National Institute of Technology. India*) Spin-Orbit Torque Magnetic Tunnel Junction based on 2-D Materials: Impact of Bias-Layer on Device Performance
4. ONLINE - S. Panwar (*Sardar Vallabhbhai National Institute of Technology. India*) Performance Optimization of Epitaxial-Layer Based Si/SiGe Hetero-junction Area Scaled Tunnel FET Label-Free Biosensors Considering Steric Hindrance
5. ONLINE - K. J. Singh (*Indian Institute of Technology Roorkee. India*). Exploring the Impact of Domain Numbers on Negative Capacitance Effects in Ferroelectric Device-Circuit Co-Design
6. P. H. Duarte (*University of Sao Paulo. Brazil*). Study of ISFET for Potassium sensing
7. S. Nagarajan (*NaMLab gGmbH. Germany*). Dopant Segregation Effects on Ohmic Contact Formation in Nanoscale Silicon
8. Y. Cao (*Xi'an Jiaotong-Liverpool University. China*). Perovskite-based optoelectronic artificial synaptic thin film transistor
9. J. García Fernández (*Universidade de Santiago de Compostela. Spain*). An accurate neural network model to study threshold voltage variability due to metal grain granularity in Nanosheet FETs
10. M. Matic (*University of Zagreb. Croacia*). Modulation of ballistic injection velocity in phosphorene nanodevices by bias and confinement effects
11. E. Miranda (*Universitat Autònoma de Barcelona. Spain*). Modeling and Simulation of Successive Breakdown Events in Thin Gate Dielectrics Using Standard Reliability Growth Models
12. F. Sabatier (*UdeS, UGA, STM. France*). Technology and design study of a 3D physics-based inductor on a FDSOI CMOS technology for quantum and RF applications
13. P. Duarte, J.A. Martino (*University of Sao Paulo. Brazil*). An enzymatic glucose biosensor using the BESOI MOSFET

14. J. Gull (*TU Wien. Austria*). Monte-Carlo Investigation of Energy Distributions in FET Channels
15. J. Martin (*Universitat Autònoma de Barcelona. Spain*). RTN and BTI statistical characterization of Ω-gate FDSOI devices at low voltages
16. M.B. Gonzalez (IMB-CNM, CSIC. Spain) Cycle-to-Cycle Variability Analysis in Ti/Al2O3-based Memristors
17. A. Tahiat (*Université de Caen Normandie. France*). Is there a limit when the access resistance impact on the extraction of key GAA NS FETs devices parameters can (not) be avoided?
18. E. Matheus de Silva (*São Bernardo do Campo, Brazil*). Junctionless Nanowire Transistors Effective Channel Length Extraction through Capacitance Characteristics
19. J. Lomonaco (*CEA, DAM, DIF. France*). TCAD Simulation Methodology of the Total Ionizing Dose Effects for PDSOI Transistor with an Unknown Hump Characteristic
20. R. Doria (*Centro Universitário FEI. Brazil*). Impact of Series Resistance on the Drain Current Variability in Inversion Mode and Junctionless Nanowire Transistors
21. A. Tahiat (*Université de Caen Normandie. France*). Novel Y-function based strategy for parameter extraction in device architectures with asymmetric S/D and LF-noise characterization of p-type Si vertical-transport nanowire FETs.
22. A. Tonon (*University of Padova. Italy*). Synthesis of MoS2 layers by sputter deposition and pulsed laser annealing
23. J. Robertson (*Cambridge University. UK*). Density Functional Analysis of Dipole Layer Voltage Shifts at High-K/Metal Gates
24. Y. Zhang. Studying the effect of back-gate on p-channel GaN heterojunction field effect transistors
25. E. di Russo (*University of Padova. Italy*). Synthesis of relaxed Ge0.9Sn0.1/Ge by nanosecond pulsed laser melting
26. U. Chatterjee (*IMEC Belgium*). A Fully Integrated HB Driver Circuit in All-GaN GANIC Technology

16:05-16:25 Coffee break

16:25-17:10 Invited talk

Luciana Capello, "Piezoelectric on Insulator structures", SOITEC (France)

17:10-18:20 Session 3. More than Moore applications. Chairs: Alex Zaslavsky and Joao Martino

17:10-17:30 F. Gámiz (*Universidad de Granada. Spain*). Simulation of BioGFET sensors using TCAD

17:30-17:50 C. Sotomayor (*ICN2. Spain*). Silicon-on-Insulator phononic source and waveguide

18:10-18:30 J. M. Rafí (*CNM-CSIC. Spain*). Ultrathin Four-quadrant Silicon Photodiodes for Beam Position and Monitor Applications

18:30-18:50 N. Kumar (*University of Glasgow. UK*). Charge Dynamics of Amino Acids Detection and the Effect of density on FinFET-based Electrolyte-Gated Sensor

20:15 Cocktail reception at Casa Joan Miret. Rambla nova 36

Thursday, May 11 2023

8:30-9:00 Registration

9:00-9:45 Invited talk

Anne Vandooren, "3D integration", IMEC (Belgium).

9:45-11:05 Session 5. Technology development. Chairs: Joris Lacord and Mikael Östling

9:45-10:05 Y. Han (*Forschungszentrum Jülich. Germany*). Improved Performance of FDSOI FETs at Cryogenic Temperatures by Optimizin0g Ion Implantation into Silicide

10:05-10:25 A. Halder (*Université catholique de Louvain. Belgium*). Comparison of Heat Sinks in Back-End of Line to reduce Self-Heating in 22FDX® MOSFETs

10:25-10:45 T. Bordignon (*STMICROELECTRONICS. France*). Computational model for predicting structural stability and stress transfer of a new SiGe stressor technique for NMOS devices.

10:45-11:05 J. Sun (*Forschungszentrum Jülich. Germany*). Low Contact Resistance of NiGeSn on n-GeSn

11:05-11:25 Coffee break

11:25-13:05 Session 6. Characterization and parameter extraction. Chairs: Denis Flandre and Chhandak Mukherjee

11:25-11:45 C. Sorin (*CNRS. France*). Detailed Comparison of Threshold Voltage Extraction Methods in FD-SOI MOSFETs

11:45-12:05 D. Bosch (*CEA LETI. France*). Electrical characterization of SOI pMOS device leakage

12:05-12:25 M. Vanbrabant (*Université Catholique de Louvain. Belgium*). Improved self-heating extraction with RF technique at cryogenic temperatures

12:25-12:45 A. Boutayeb (*8 STMicroelectronics Crolles. France*). Extracting Edge Conduction around Threshold in mesa-isolated SOI MOSFETs

12:45-13:05 Y. Yifan (*Kansai University. Japan*). Detailed analysis of electrical components on a layered wafer with an ac pseudo-MOS method

13:10-14:45 Lunch

14:45-15:30 Invited talk.

Stefan Lischke, "Photonic BiCMOS technology - enabler of high-speed monolithic EPIC", Leibniz-Institute for High Performance Microelectronics (Germany).

15:30-16:50 Session 7. Memory and memristor devices. Chairs: Pierpaolo Palestri and Cor Claeys

15:30-15:50 C. Valdivieso (*Universitat Autònoma de Barcelona. Spain*) Resistive Switching like-behaviour in FD-SOI Ω-gate transistors

15:50-16:10 M. Bendra (*Technical University Vienna. Austria*). A Multi-Level Cell for Ultra-Scaled STT-MRAM Realized by Back-Hopping

16:10-16:30 P. Wisniewski (*Warsaw University of Technology. Polen*). Study of Silicon-Oxide RRAM Devices Based on Complex Impedance Spectroscopy

16:30-16:50 P. Dimitrakis (*INN-NCSR Demokritos. Greece*). Silicon Nitride resistance switching MIS cells doped with Silicon atoms

16:50-17:10 Coffee break

20:30 Gala dinner. Restaurant Nàutic de Tarragona

Friday, May 12 2023

9:20-10:05 Invited talk

Muhammad Nawaz, "SiC devices for power electronics; performance, issues and challenges", Hitachi Energy (Sweden)

10:05-11:05 Session 8. Novel device technologies. Chair: Sorin Cristoloveanu

10:05-10:25 J. Ida (*Kanazawa Institute of Technology. Japan*). First fabrication results of Steep Subthreshold Slope “Dual-Gate PN-Body Tied SOI-FET

10:25-10:45 J. H. Quintino Palhares (*STMicroelectronics. Université Grenoble Alpes. Canada*). A tunable 28nm FD-SOI crossbar output circuit for low power analog SNN inference with eNVM synapses

10:45-11:05 A. Rodríguez-Iglesias (*IMB-CNM-CSIC. Spain*). Micro-thermoelectric generators based on Si enhanced by heat sink integration

11:05-11:25 Coffee break

11:25-13:05 Session 9. Modeling and simulation. Chairs: Francisco Gámiz

11:25-11:45 A. Mounir (*Rovira i Virgili University. Spain*). Compact I-V Model of Back-Gated Monolayer MoS2 FETs with a Bias-Dependent Mobility.

11:45-12:05 C. Römer (*Technische Hochschule Mittelhessen. Germany*). Compact Modeling of Schottky Barrier Field-Effect Transistors at Deep Cryogenic Temperatures

12:05- 12:25 N. Zerhouni-Abdou (*CEA Leti. France*). Undoped junctionless EZ-FET: model and measurements

12:25-12:45 N. Dersch (*Technische Hochschule Mittelhessen. Germany*). Efficient Circuit Simulation of a Memristive Crossbar Array with Synaptic Weight Variability

12:45-13:05 Y. Huang (*IMECAS. Belgium*). C-V Measurement and Modeling of Double-BOX Trap-Rich SOI Substrate

13:10-14:45 Lunch

14:45-16:05 Session 10. Nanowires, nanosheets and quantum dots. Chairs: Luca Selmi and Farzan Gity

14:45-15:05 M. de Souza (*Centro Universitario FEI. Brazil*). Experimental Assessment of Gate-Induced Drain Leakage in SOI Stacked Nanowire and Nanosheet nMOSFETs at High Temperatures

15:05-15:25 C. Pereira de Silva (*UNESP - Sao Paulo State University. Brazil*) Evaluation of n-type gate-all-around vertically-stacked nanosheet FETs from 473 K down to 173 K for analog applications

15:25-15:45 P. Galy (*Stmicroelectronics. Brazil*). Simulation process flow for the implementation of industry-standard FD-SOI quantum dot devices

15:45-16:05 Y. Wang (*University of Bordeaux. France*). Evidence of Trapping and Electrothermal Effects in Vertical Junctionless Nanowire Transistors

16:05-16:20 Conference closing